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A Fully-Integrated 1μW/Channel Dual-Mode Neural Data Acquisition System for Implantable Brain-Machine Interfaces

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***Abstract*— This paper presents an ultra-low power mixed-signal neural data acquisition (MSN-DAQ) system that enables a novel low-power hybrid-domain neural decoding architecture for implantable brain-machine interfaces with high channel count. Implemented in 180nm CMOS technology, the 32-channel custom chip operates at 1V supply voltage and achieves excellent performance including 1.07μW/channel, 2.37/5.62 NEF/PEF and 88dB common-mode rejection ratio (CMRR) with significant back-end power-saving advantage compared to prior works. The fabricated prototype was further evaluated with *in vivo* human tests at bedside, and its performance closely follows that of a commercial recording system.**

I. INTRODUCTION

Restoration of neurological functions impaired by spinal cord injury necessitates implantable brain-machine interfaces (BMIs), capable of neural signal acquisition, processing, and wireless connectivity to external base-station and end-effectors. While electrocorticography (ECoG)-based BMIs provide superior signal stability, electrode longevity and spatial resolution/area coverage for accurate decoding of neural activity, the overall power dissipation needs to be minimized to allow prolonged battery life which is a critical aspect of biomedical implants. Existing neural decoding architecture for implantable BMIs is primarily based on conventional power-hungry brain signal acquisition and processing approaches, which are ill-suited for high channel-count systems [1]. Shown in Fig. 1, a standalone data acquisition (DAQ) captures neural signals of varying amplitudes across a wide range of frequencies (near DC up to 1 kHz) and provides digitized samples to a back-end processor for decoding purposes. However, the relevant physiological neural information, such as movement intentions, is typically encoded within a fraction of frequency range (e.g., high-γ band) whose content requires significantly less dynamic range and bandwidth compared to the raw neural signal. As such, conventional DAQ is bound to operate with an excess dynamic range and bandwidth that result in an unduly high data throughput, placing a significant power and computing burden on digital signal processor (DSP). Recent works do not address this prominent data-processing power bottleneck for massive channel-count systems, including several neural recording architectures based on capacitively-coupled

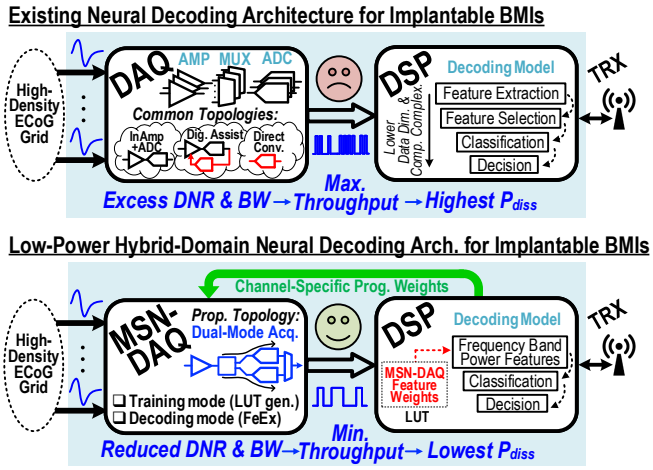

Fig. 1. Conventional and proposed neural decoding architectures for high channel-count implantable brain-machine interfaces.

InAmp+ADC [2], DC-coupled digitally-assisted amplifier [3] and direct conversion (time-based [4], delta-sigma [5]) schemes.

Inspired by our work in [6], the proposed mixed-signal neural DAQ (MSN-DAQ) enables a novel low-power hybrid-domain neural decoding architecture for implantable BMIs by adopting dual-mode acquisition that is intended for distinct use in training and decoding procedures, with the latter accounting for the majority of operation time. In training mode, raw neural signals are collected by MSN-DAQ during a set of clinical trials and transmitted to an external base-station where decoder training takes place offline [7], [8]. While training helps improve decoding accuracy and provides a means of calibration and validation, it primarily involves data collection with increased bit-resolution and sampling rate, further justifying the dual-mode acquisition. Once the decoder's performance is optimized, identified features and their corresponding weights are computed in a lookup table to be transferred to DSP and subsequently applied to the channel-specific programmable weights on MSN-DAQ, marking the transition to decoding mode. Similar to [6], feature extraction is performed in analog domain using the stored weights, which facilitates the digitization with minimum required bit-resolution and sampling rate. Hence, the DSP power dissipation is significantly relaxed. Furthermore, no computationally-expensive algorithm needs to be executed on DSP for decoding in this proposed framework, and therefore, the back-end's complexity overhead remains relatively low with increasing number of channels, a highly desired attribute for real-time operation in implantable BMIs with multiple functionalities.

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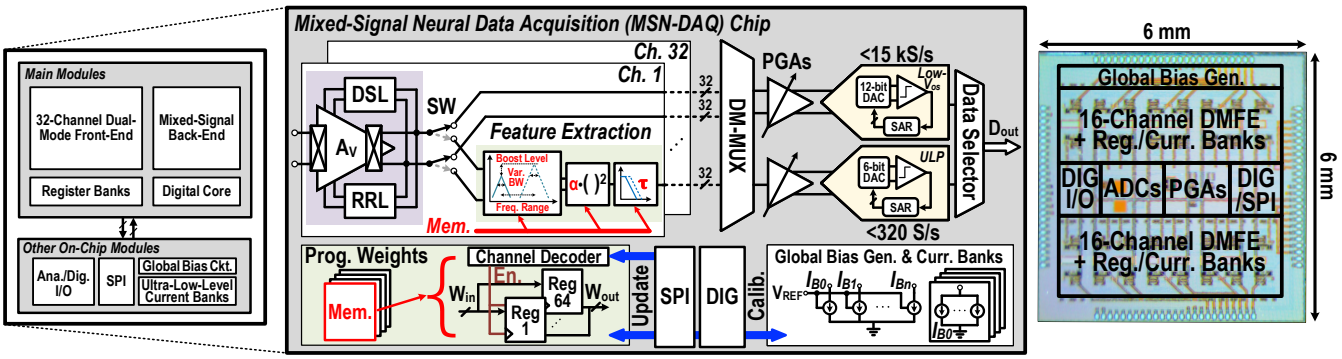

Fig. 2. System architecture of the mixed-signal neural data acquisition (MSN-DAQ) chip and a micrograph of its fabricated prototype.

The rest of this paper is organized as follows: Section II describes the proposed MSN-DAQ system and its circuit implementation. Experimental results including electrical and *in vivo* measurements are presented in Section III, followed by concluding remarks in Section IV.

II. PROPOSED MIXED-SIGNAL NEURAL DAQ

Fig. 2 shows the top-level system block diagram of MSN-DAQ. The main modules include a 32-element dual-mode front-end array with register banks to store channel-specific programmable weights, mixed-signal back-end consisting dual-mode multiplexer (DM-MUX), programmable gain amplifiers (PGAs), analog-to-digital converters (ADCs) with distinct bit-resolution and bandwidth requirements for training and decoding modes, and a digital core. Other on-chip blocks include serial peripheral interface (SPI), bias circuitry for global current generation, digitally-controlled ultra-low-level current banks and analog/digital input-output (I/O) modules.

A. Dual-Mode Front-End and Analog Interface Circuits

The dual-mode front-end includes a newly-added low-noise, folded-cascode chopper-stabilized amplifier array. Shown in Fig. 3 is the closed-loop amplifier incorporating two auxiliary loops across the output and folding nodes: (a) DC servo loop to further attenuate low-frequency signals and minimize the output offset, and (b) ripple reduction loop to minimize chopping ripples introduced by up-modulated voltage offset of the input stage, $G_{m,1}$. Given that the chopping mechanism eliminates the mismatch effect of transistors, high common-mode rejection ratio (CMRR) can be achieved. To further improve CMRR, input capacitors were adequately sized to reduce mismatch and the common-mode to common-mode attenuation was notably increased by using an input-injecting common-mode feedback (CMFB) network, which remarkably improves the source impedance by an additional loop gain factor.

Depending on acquisition mode, raw neural signal or extracted neural features are time-multiplexed and further amplified by the respective PGA. Since raw signals contain higher dynamic range and bandwidth, the required settling time prior to digitization is significantly shortened. A higher unity gain-bandwidth product required in training mode is achieved by increasing the transconductance, resulting in higher power consumption in this mode. Conversely, neural features do not suffer from this problem, and thus, the PGA consumes significantly less power in decoding mode.

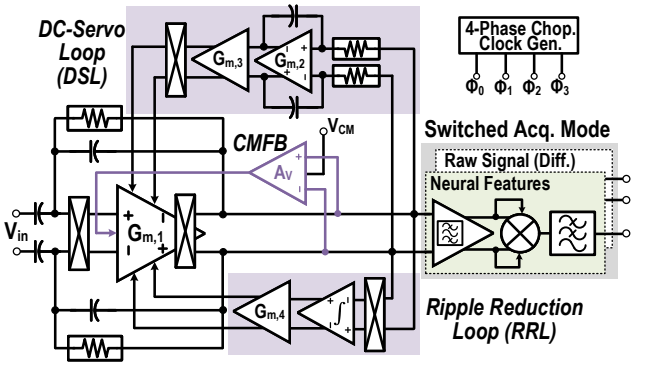

Fig. 3. Schematic details of dual-mode front-end, incorporating DC-servo loop, ripple reduction loop and common-mode feedback.

B. Successive Approximation Register ADCs

To meet the stringent power requirements of neural data acquisition, successive approximation register (SAR) ADC is chosen. Shown in Fig. 4, the differential 12-bit SAR-ADC includes a V_{CM}-based binary-weighted capacitive digital-to-analog converter (DAC) array, a multi-stage offset-canceling comparator and a compact modular non-redundant SAR logic and control with minimum circuit overhead. The digitization begins with top-plate sampling of the amplified differential input signal, followed by the energy-efficient bit-cycling that is accomplished by V_{CM}-based switching scheme. To satisfy the required resolution, a combination of circuit and layout techniques have been utilized. Most notably, the comparator employs three-stage pre-amplification with output offset cancellation (OOS) to minimize the input-referred voltage offset and the kickback noise introduced by the regenerative latch. Moreover, twisted differential signaling is applied between the DAC and the comparator to suppress common-mode noise (Fig. 4). To implement the SAR algorithm, a compact modular digital circuity based on non-redundant logic is used. Illustrated in Fig. 4, the entire SAR logic consists of only 12 MUXed D-flipflops and 11 OR gates. Moreover, a unique control circuitry (shaded in light blue) – consisting of only 1 D-flipflop, 1 inverter and 2 AND gates for each bit – is implemented to accommodate the V_{CM}-based switching procedure. The working principle is as follows: Initially, each D-flipflop in the control circuitry

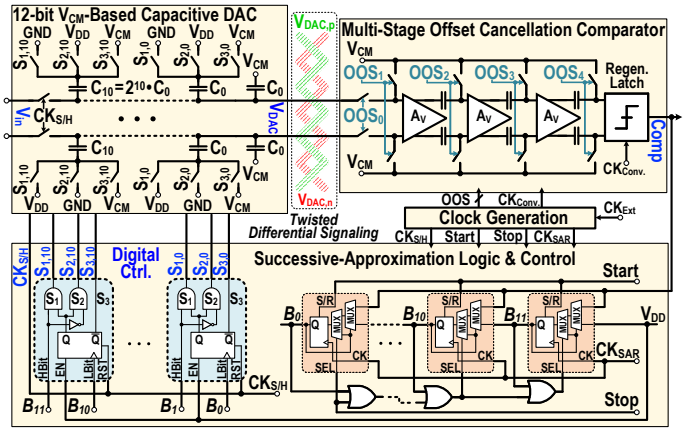

Fig. 4. Schematic details of SAR-ADC, highlighting the digital logic and control circuitry for V_{CM}-based capacitive DAC.

is reset by $CK_{S/H}$ during the sample and hold operation. Thus, all S_3 switches are enabled in the capacitive DAC, connecting the bottom plate of each capacitor to the common-mode voltage (V_{CM}). Next, SAR logic produces a leftward-propagating pulse that is sequentially captured by each stage in the shift register. Each in-between interval lasts for one clock period of CK_{SAR} and represents a comparison window. During each interval, one bit is resolved at a time and the result is stored in the corresponding MUXed D-flipflop. Starting with the most significant bit, the direction of binary search is determined by the stored value at the end of each comparison window. Given the inherent sequential operation of SAR algorithm within comparison windows, each control D-flipflop detects the transition instances and generate the necessary control signals by a simple combinational circuit. Depending on the outcome, the appropriate DAC switch (S_1 or S_2) is activated at the beginning of each comparison window immediately after S_3 is turned off. The detection and control signal generation continue until all bits have been resolved, and a new conversion takes place.

III. EXPERIMENTAL RESULTS

A. Electrical Measurements

MSN-DAQ chip achieves a measured 42.5-dB minimum closed-loop gain, 1.03 μV_{rms} input-referred noise (2-200 Hz), 2.37 noise efficiency factor (NEF), 5.62 power efficiency factor (PEF) at 1V supply voltage, and 88-dB average CMRR for a maximum 10mVpp interference within 50-160 Hz range. Fig. 5(a) shows the measured frequency response of MSN-DAQ across 3 neighboring channels and different gain modes for one channel. Based on measured FFT of the 12-bit SAR-ADC output for 193.17-Hz tone (i.e., upper edge of the frequency band) at maximum sampling rate of 15kHz, the ENOB, SFDR, and SNDR are 10.5, 65.2 dB, 64.78 dB, respectively, as depicted in Fig. 5(b).

B. Biomedical Testing and In Vivo Measurements

To further validate MSN-DAQ operation within a clinical context, neural recordings were carried out on an epileptic patient with implanted ECoG grids. The study was approved by the Institutional Review Board of the Rancho Los Amigos National Rehabilitation Center and the University of

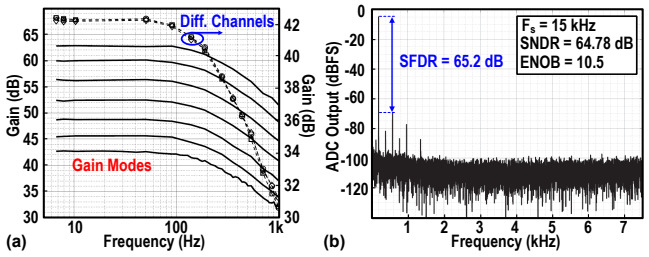

Fig. 5. (a) MSN-DAQ measured frequency response and (b) ADC measured output power spectrum.

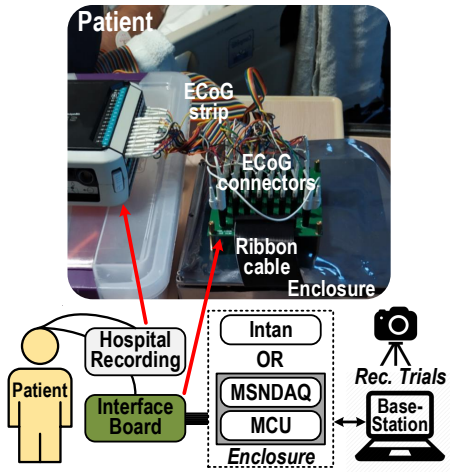

Fig. 6. Hospital experiment setup, including the custom chip (MSN-DAQ) and commercial system (Intan).

California, Irvine. Fig. 6 illustrates the experiment setup with connections between the implanted ECoG girds and the recording systems, including hospital clinical acquisition (i.e., Natus® Quantum™) and MSN-DAQ placed in a shielding enclosure. A similar setup was reproduced for the commercial Intan recording system (RHD2000), substituting Intan for MSN-DAQ to allow comparison with the custom chip. The raw neural data were acquired from 32 anteriorly placed electrodes over M1 (MG1-32) for ten 14-second idle periods and ten 14-seconds move periods during a hip flexion task. Fig. 7(a) shows a sample of acquired time-series data from three electrodes over the motor leg area that exhibited behavioral modulation. Fig. 7(b) show the spectrogram demonstrating μ-β power modulations for a pair of idle/move trials. After further statistical analysis of all the recorded trials, the power for idle and move states within each frequency band were plotted for both MSN-DAQ and Intan recording systems – as depicted in Fig. 8 – which exhibit similar distinguishable difference. Given that placement of ECoG grid was dictated by the patient's clinical needs, the highly-localized gamma activity correlated to hip flexion appeared to be less prominent, particularly for high-γ band which did not attain the expected distinguishable SNR range that have been previously observed in our prior works. Thus, the extracted high-γ features in decoding mode did not contain meaningful information regarding idle/move states. Nevertheless, to validate the operation in decoding mode, ECoG data containing high-γ modulations from previous hospital experiments were fed to MSN-DAQ by a high-resolution waveform generator. The extracted power enve-

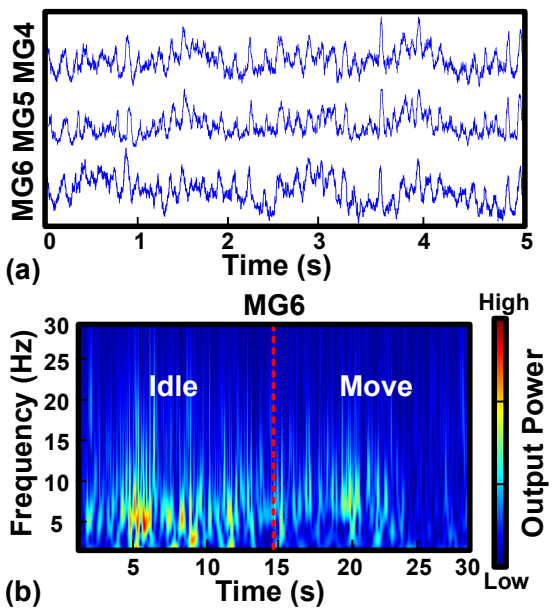

Fig. 7. (a) ECoG time-series sample data from motor grid (MG) electrodes and (b) spectrogram of raw ECoG from MG6, acquired by MSN-DAQ.

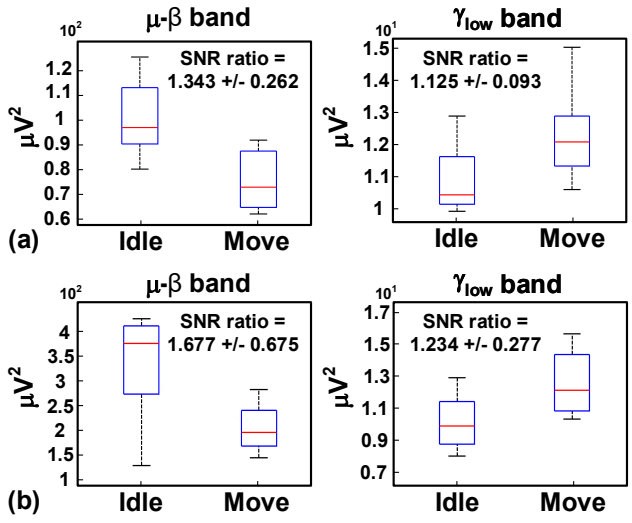

Fig. 8. Box plots showing signal-to-noise power ratio (SNR) between idle and move states from (a) MSN-DAQ and (b) Intan recording system.

lope from an ECoG channel exhibiting high-γ modulation in response to an upper extremity movement task is shown in Fig. 9.

IV. CONCLUSION

A dual-mode mixed-signal neural data acquisition was presented. The 180nm CMOS chip enables a novel low-power hybrid-domain neural decoding architecture for implantable BMIs that could achieve significant power saving in high-channel count systems. In addition to electrical measurements, the prototype has been validated in a hospital setting with real-time human ECoG recording. A comparison with the most relevant prior works in Table I shows that the proposed MSN-DAQ achieves excellent CMRR and noise performance at lowest power consumption per channel.

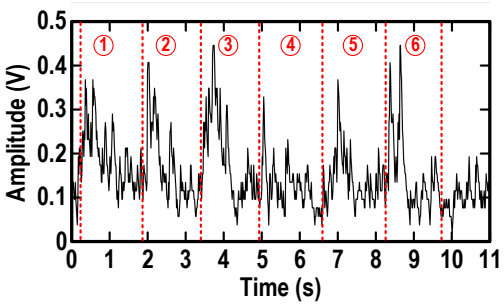

Fig. 9. Extracted high-γ features in decoding mode, exhibiting power modulations during six consecutive elbow flexion and extension periods.

TABLE I
PERFORMANCE COMPARISON

	JSSC'15 [3]	TBCAS'18 [9]	JSSC'19 [4]	TBCAS'20 [10]	**This Work**
Tech. (nm)	65	180	180	65	**180**
Supply (V)	0.5	1.8	1.2	0.5, 2.5	**1**
Channel	64	16	4	64	**32**
Power/Ch. (μW)	2.3	3.26	3.9	2.98	**1.07**
BW (Hz)	1-500	0.59-117	200	1-1k	**2-200**
IRN (μV_{rms})	1.23	2.02	1.3	1.66	**1.03**
NEF	3.7	3.36	4.9	2.21	**2.37**
PEF	6.9	20.32	28.81	-	**5.62**
CMRR (dB)	88	67.1	>75	76	**88**
ADC Res.	15	10	-	16	**12**
ENOB	-	7.8	13.2	15.7	**10.5**

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