2021 43rd Annual International Conference of the
IEEE Engineering in Medicine & Biology Society (EMBC)
Oct 31 - Nov 4, 2021. Virtual Conference

A 100-V Withstanding Analog-Front-End for High-Resolution Intravascular Ultrasound Imaging

Wangbo Chen[1,2], Aaron Fleischman[3], and Steve J.A. Majerus[1], *Senior Member, IEEE*

***Abstract*—Intravascular Ultrasound ultrasonic imaging (IVUS) can microscopically image blood vessels and reveal tissue layers from within the blood vessel lumen. It has high tissue penetration ability for lesion classification and can image through blood. Compared to optical techniques, however, IVUS has lower resolution arising from low acoustic bandwidths which cannot resolve sharp edges. The presented 100-V withstanding Analog-Front-End (AFE) was developed to enable a high resolution, low cost IVUS system using a high-bandwidth focused polymer transducer with 40-MHz center frequency. The fabricated AFE interfaced with the transducer with minimal insertion loss, could withstand and duplex 100-V high voltage pulses and echo signal, and had a total signal chain gain of 9.8 dB. The AFE achieved a signal-to-noise ratio (SNR) of 20.1 dB including the insertion loss of the high-impedance transducer. AFE SNR was limited by input impedance required for high-voltage pulse clamping circuitry, but was sufficient for IVUS echo reception.**

***Clinical Relevance*— This work has the potential to enable much higher resolution, and potentially cheaper, IVUS imaging in blood vessels by integrating low-cost acoustic transducers with interface amplifiers directly on the catheter.**

I. Introduction

Intravascular Ultrasound Imaging (IVUS) is a technique for imaging coronary and peripheral blood vessels. IVUS can image through blood and provide high imaging penetration for lesion identification and classification[1], [2]. While IVUS can provide depth information on layers of tissue, it has lower resolution than other techniques such as optical coherence tomography[3]. Expanding the acoustic bandwidth of IVUS enables tissue harmonic imaging to determine tissue composition during imaging and increases the axial resolution; and focusing the transducer improves lateral resolution. High-bandwidth polymer ultrasonic transducers that are easy to shape are ideal for this application but require and front-end interface amplifiers due to the high output impedance of these transducers[4].

This aims to improve high resolution, low-cost IVUS systems using high frequency, high bandwidth piezoelectric micro-machined ultrasonic transducers (PMUTs). The system will have superior resolution to image small critical structures while still having high soft tissue penetration for soft plaque evaluation. Compared to other IVUS transducers, PMUTs are potentially cost effective because they are generally fabricated from piezoelectric films such as poly[(vinylidenefluoride-co-trifluoroethylene] (PMUT-TrFE).

PMUT-TrFE, compared to conventional ceramic transducers and capacitive micro-machined ultrasonic transducers (CMUT), has higher bandwidth and output impedance [5]–[10]. Hence, PMUT-TrFE transducers cannot be directly connected to the conventional 1 mm diameter, 1.5 m, 50 Ω coaxial cable without significant insertion loss. To buffer the high impedance transducer signal, an Analog Front End (AFE) Application Specific Integrated Circuit (ASIC) was designed to interface with a PMUT-TrFE transducer. The AFE ASIC was developed to withstand high-voltage pulses during imaging, while retaining low noise amplification of acoustic echoes from tissue targets.

The AFE was designed to be mounted at the tip of the catheter next to the PMUT-TrFE transducer. Therefore, the ASIC had a width of 0.85 mm allowing for flip-chip bonding. The ASIC was twice as long as needed to include test circuits. Here, we present preliminary bench characterization data that the ASIC can interface with the PMUT-TrFE transducer, withstand a 100-V pulse, pre-amplify, and buffer the echo signal with appropriate post-high-voltage-pulse recovery time. We have also shown that the fabricated silicon could be integrated with a PMUT-TrFE transducer on a miniaturized PCB that fits within a standard 1mm catheter (Fig. 1).

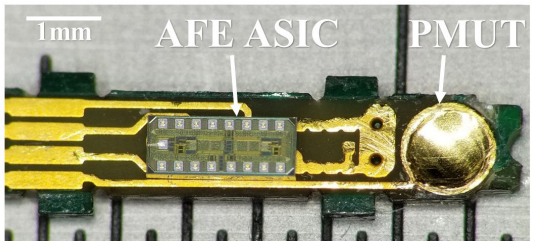

Fig. 1. The AFE ASIC was designed for co-bonding with a PMUT-TrFE. Here, the ASIC is flipped over to help visualize the circuitry and bondpads.

II. Polymer Micro-Machined Ultrasonic Transducer

A high-frequency transducer improves spatial resolution in ultrasonic imaging. The proposed IVUS system operates at 40 MHz, with sufficient bandwidth to capture the 2nd harmonic at 80 MHz and a sub-harmonic at 20 MHz. This wide bandwidth allows echo data collection at the harmonic frequencies for image sharpening.

* This work was supported by the US Dept. of Veterans Affairs Advanced Platform Technology Center and Case Western Reserve University.

W. Chen and S.J.A. Majerus are with the [1]Advanced Platform Technology Center, Louis Stokes Cleveland VA Medical Center, Cleveland, OH 44106 USA (e-mail: steve.majerus@va.gov).

W. Chen is with the [2]Electrical, Computer, and Systems Engineering Department, Case Western Reserve University, Cleveland, OH 44106 USA.

A. Fleischman is with the [3]Department of Biomedical Engineering, Cleveland Clinic Lerner Research Institute, Cleveland Clinic, Cleveland, OH 44106 USA.

A PMUT-TrFE transducer was designed to resonate at 40 MHz and spherically focused using a custom forming tool. The transducer impedance was measured and modeled as a 2.2 pF capacitor with 30 kΩ leakage resistance. Acoustic modeling estimated the transducer SNR to be 88 dB [11], however, due to the high impedance, this SNR would be reduced by 19 dB in a 50 Ω system. Co-locating an AFE close to the PMUT was shown to improve SNR by 20 dB previously [5]. Therefore, we adopted the same approach in which a transducer-scale AFE is mounted at the end of the IVUS catheter to preserve PMUT SNR and bandwidth.

III. Analog Front End Interface

The AFE duplexes the high voltage pulses and amplifies and buffers the echo signals. A shunt/series-duplexer topologies was considered because modern integrated fabrication processes do not provide high voltage FETs to withstand the pulsing voltage [12]. Instead, an active limiter clamps the input voltage under the allowable voltage level of 7 V peak (drain-source breakdown voltage of the process). This topology allowed the ASIC to be fabricated with standard low-voltage processes with high breakdown voltage metal-insulator-metal capacitors.

The active limiter was designed based on the current flow into the low voltage part of the circuit, namely the amplifier and buffer. In the fabricated design, a series-duplexer topology was chosen over the shunt-duplexer topology (Fig. 2) because shunt duplexers amplify the noise of the IVUS pulser when it is not pulsing. The series duplexer also has a significantly lower clamping current, minimizing the size of the limiter parasitic impedance. In this work, we used a series-duplexed AFE consisting of a high voltage coupling capacitor, an LNA, and an active limiter.

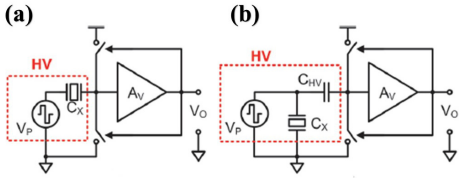

Fig. 2. (a) Shunt-duplexer, and (b) series-duplexer, both using an active limiter.

A. High Voltage Coupling Capacitor

The value of the high voltage capacitor C_{HV} was optimized for signal chain gain and SNR by selecting the size of the high voltage coupling capacitor [12]. C_{HV} increases input impedance to limit current during high voltage pulsing, without overly loading the transducer during echo recovery. However, while a large coupling capacitor reduces insertion loss, it increases clamping current during pulsing cycles. This increases the size of limiter transistors, which reduces signal gain. Therefore this amplifier topology has a process-dependent optimum C_{HV} based on the transducer capacitance [12].

The AFE was designed for the OnSemi I3T80 process, which offers metal-insulator-metal (MIM) capacitors rated to 50 V. Two high voltage capacitors were put in series to implement a 100-V tolerant coupling capacitor with substrate-coupled parasitic capacitance (Fig. 3). The ratio of parasitic capacitance to high voltage capacitor was modeled as $\kappa = C_{HVpar}/C_{HV}$. The parameter κ was extracted from capacitance tables, and for the I3T80 process $\kappa = 15\%$.

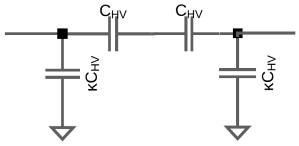

Fig. 3. Parasitic model of the coupling capacitor. Parasitic capacitance κC_{HV} appears at the LNA input, decreasing its gain and bandwidth.

B. Active Limiter

The active limiter clamps the voltage during the pulsing period below the FET gate breakdown voltage [12]. The active limiter used two large transistors with drains tied to the supply rails. During high voltage pulsing, feedback inverters sense LNA output voltage and activate the limiter switches (Fig 4). This feedback limits the LNA output voltage swing to approximately one MOS threshold voltage.

The large active limiter transistors contribute significant input parasitic capacitance to the LNA. The minimum size of active limiter transistors was related to coupling capacitor size and maximum edge rate by a process dependent parameter γ,

$$\gamma = {C_{LIM}}/{\frac{1}{2}C_{HV}} = \alpha\left(\frac{dV_p}{dt}\right)_{max} \quad (1)$$

where V_p is the pulsing voltage, α is the ratio of parasitic capacitance to limiter transistor current capability. By simulation, α = 9.3 pF/A and γ = 6.9 was calculated for the I3T80 process. These values were used for SNR optimization of the amplifier.

C. Low Noise Amplifier and Buffer

The LNA pre-amplifies and sets the bandwidth of the echo signal. It was implemented using a self-biased push-pull topology with resistive feedback (Fig. 4). Feedback resistance R_f set the amplifier's gain. The combination of feedback capacitance C_f—the sum of C_{gd} of the two amplifier transistors—and R_f, set the LNA bandwidth.

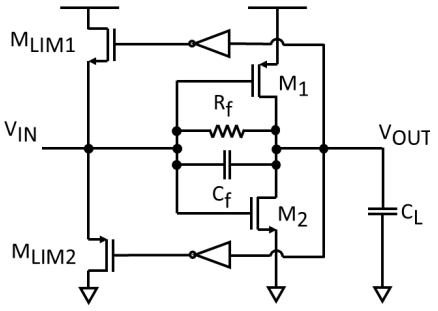

Fig. 4. The LNA was implemented using a self-biased push-pull topology with resistive feedback R_f. Two feedback inverters sense the output voltage and switch on or off the limiter transistors.

With process dependent parameter κ and γ, we selected C_{HV} by optimizing the trade-off between input signal amplitude and amplifier gain (Fig. 5). With a constraint of minimum signal gain of 3 V/V, the SNR was maximized with $C_{HV} = 2 - 5pF$. The design used $C_{HV} = 3.45\ pF$ to account for fabrication tolerance.

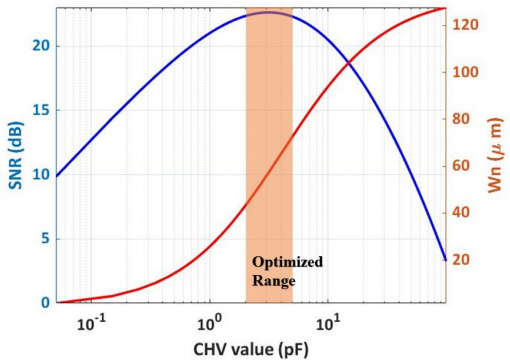

Fig. 5. Total AFE SNR and LNA NMOS width vs. C_{HV} value. The fabricated design used C_{HV} = 3.45 pF and LNA NMOS width of 60 µm.

IV. Results

The AFE ASIC was fabricated in the OnSemi I3T80 0.35-µm process (Fig. 6). Each chip had a full AFE, and isolated AFE sections for individual testing (Fig. 7). The chip (including test circuits) was suitable for integration with the PMUT transducer on a 1 mm wide PCB within a catheter (Fig. 7).

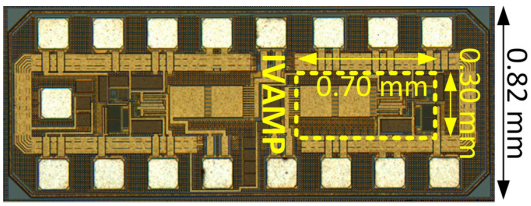

Fig. 6. Die photograph of the fabricated AFE ASIC. The active area for the AFE including HV capacitor was 0.30 × 0.70 mm, labeled as IVAMP.

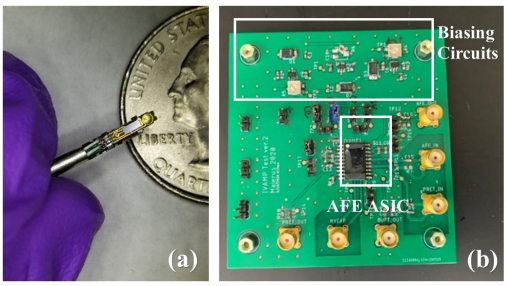

Fig. 7. (a) AFE ASIC and PMUT-TrFE integrated on a miniaturized PCB which was mounted on the tip of a standard 1 mm catheter. (b) Test board used to characterize the AFE performance and pulse tolerance.

A. High Voltage Capacitor Testing

Using an impedance analyzer (Agilent 4395A, Agilent Technology), we measured the coupling capacitor (C_{HV}) for two chips. The values of 3.46 pF and 3.66 pF were close to the designed value and well within the optimized range.

During imaging, the 100-V high voltage pulses could potentially stress the capacitors. To determine capacitor stability, we subjected an unpulsed coupling capacitor to 100-V pulses and measured the capacitor value over 2M pulse cycles (Table I). Recorded data showed no degradation of the coupling capacitors under high voltage pulses.

TABLE I. CHV Value After 100-V Pulsing

Cycles Pulsed	10k	100k	500k	1M	2M
C_{HV} Measured (pF)	3.46	3.40	3.46	3.44	3.46

B. Pulse Recovery

IVUS imaging requires the amplifier to recover quickly post-pulsing to receive the small signal echo from tissue. To image blood vessel walls only 0.5 mm away from the tip of the catheter, the amplifier must recover within 667 ns after pulsing, based on the speed of sound in blood.

The LNA recovery time was tested with a commercial pulser (Avtech AVB1-3-C, Avtech Electrosystems). A 100-V high voltage, 40 MHz monocycle pulse was applied to the input of the AFE to test the clamping ability of the active limiter and the post-pulse-recovery time of the amplifier. As a result, the amplifier's output voltage was kept well below breakdown voltage, and the amplifier recovered ~500 ns after pulsing (Fig. 8). The measured recovery time was significantly less than 667 ns and suitable for IVUS imaging.

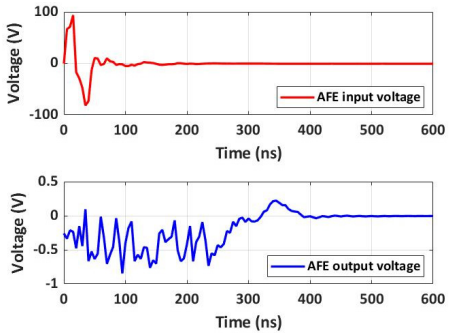

Fig. 8. AFE input and output voltage during a pulsing cycle. The AFE input remained below breakdown voltage, and the AFE recovered within 500 ns.

C. Signal Amplifier Testing

The AFE had an unloaded gain of 15 dB (Agilent 4395A, Agilent Technology) and a -3 dB bandwidth of 110 MHz. When loaded with 50 Ω, the AFE had a -3 dB bandwidth of 92 MHz, and a unity-gain bandwidth of 225 MHz (Fig. 9).

To calculate the total signal chain gain, the insertion loss (IL) between the PMUT-TrFE and AFE was first measured as IL ≅ 5.2 dB at 40 MHz. Therefore, the loaded total AFE gain was 9.8 dB at 40 MHz. The equivalent AFE SNR was 20.1 dB assuming a transducer-referred input signal of 1 mV. This exceeded the reported SNR and bandwidth for several state-of-the-art capacitive micromachine ultrasonic transducer (CMUT) based IVUS systems [7], [13].

The output impedance of the AFE buffer was designed to be 50 Ω. The output impedance was measured to be 53.7 Ω and 51.7 Ω for both chips tested. This enabled the AFE to directly connect to 50 Ω transmission line coaxial cables used in IVUS systems.

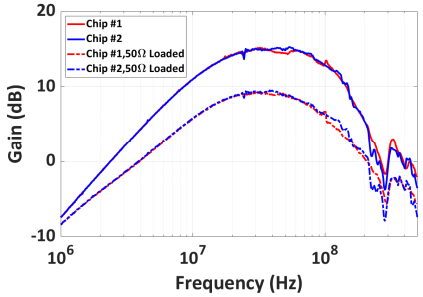

Fig. 9. S21 measurements of the AFE showed a gain of ~9 dB with a 50 Ω load. The 92 MHz amplifier bandwidth (10 – 102 MHz) is sufficient for wideband IVUS imaging using the PMUT-TrFE.

TABLE II. SUMMARY OF AFE TESTING RESULTS

Parameters	*Simulated*	*Tested*
High Voltage Capacitor, C_{HV}	3.45 pF	3.46 pF
Total Signal Chain Gain (Unloaded)	4.04 V/V	3.13 V/V
Bandwidth	6 – 107 MHz	10 – 120 MHz
Integrated output-Referred Noise	335 μV_{RMS}	384 μV_{RMS}
Output impedance	50 Ω	51.7 – 53.7 Ω
Transducer insertion loss at 40 MHz	-	5.2 dB
Signal to Noise Ratio[a]	21.7 dB	20.1 dB
Pulse Recovery Time	250 ns	500 ns

[a]Assuming 1 mV acoustic echo received by PMUT during imaging

D. Pulse-Echo Testing

To demonstrate the AFE ASIC working with the PMUT-TrFE transducer, a pulse-echo test was designed (Fig. 11). A 0.8-mm PMUT-TrFE was mounted on a small PCB, and immersed in water in a beaker. The test PMUT-TrFE was positioned so that the bottom of beaker was one focal length away. The test PMUT-TrFE board was connected to the input of the AFE using 50 Ω coaxial cable. A commercial IVUS pulser was connected to the input of the AFE and PMUT to provide a high voltage 40 MHz monocycle pulse. Measurements were taken with a sampling oscilloscope (Agilent DSO-X 3054A Oscilloscope, Agilent Technology) at the input of AFE (attenuated by 48 dB to protect the oscilloscope from direct pulsing), and the output of AFE.

The test successfully demonstrated that the AFE ASIC interfaced well with the PMUT (Fig. 12). It duplexed high voltage pulses and echo signals, and amplified and buffered the echo signal into a 50 Ω system. This basic test demonstrated pulse-echo transmission and reception with a received signal amplitude of about 100 mV.

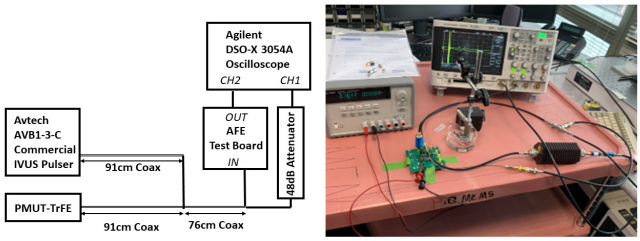

Fig. 10. (a) Block diagram and (b) setup for IVUS pulse-echo test.

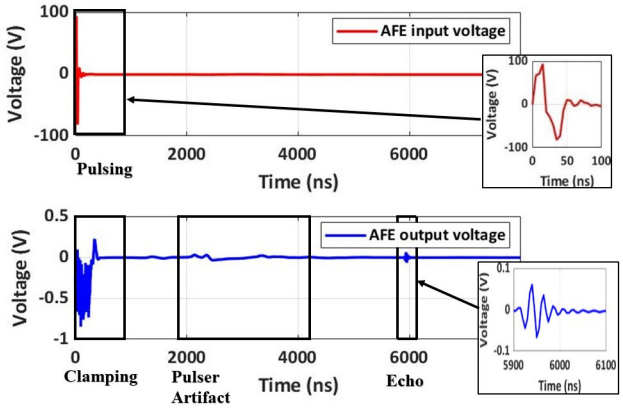

Fig. 11 The pulse-echo test captured voltages at the input and output the AFE. This demonstrated active clamping of the 100-V excitation pulse and subsequent reception of the acoustic echo at the focal length of the 0.8-mm PMUT.

V. CONCLUSION

PMUT-TrFE transducers offer wide bandwidth IVUS imaging but require special consideration due to the high impedance and high-voltage pulsing requirements. Custom AFE ASICs as we demonstrated can be co-located with the transducer, enabling functionality in a 50 Ω system. The fabricated AFE ASIC withstood conventional 100-V high voltage pulses while recovering quickly enough to amplify echoes from close targets. Future efforts for the 100-V withstanding AFE include catheter integration with the PMUT-TrFE and further reduction of ASIC dimensions for improved PCB mounting.

REFERENCES

[1] A. Nair, B. D. Kuban, E. M. Tuzcu, P. Schoenhagen, S. E. Nissen, and D. G. Vince, "Coronary Plaque Classification With Intravascular Ultrasound Radiofrequency Data Analysis," *Circulation*, vol. 106, no. 17, pp. 2200–2206, Oct. 2002.

[2] S. K. Mehta, J. R. McCrary, A. D. Frutkin, W. J. S. Dolla, and S. P. Marso, "Intravascular ultrasound radiofrequency analysis of coronary atherosclerosis: an emerging technology for the assessment of vulnerable plaque," *Eur. Heart J.*, vol. 28, no. 11, pp. 1283–1288, Jun. 2007.

[3] M. Okubo *et al.*, "Tissue Characterization of Coronary Plaques Comparison of Integrated Backscatter Intravascular Ultrasound With Virtual Histology Intravascular Ultrasound," *Circ. J.*, vol. 72, no. 10, pp. 1631–1639, 2008.

[4] A. Fleischman, R. Modi, A. Nair, J. Talman, G. Lockwood, and S. Roy, "Miniature high frequency focused ultrasonic transducers for minimally invasive imaging procedures," in *Sensors and Actuators, A: Physical*, Jan. 2003, vol. 103, no. 1–2, pp. 76–82.

[5] A. Fleischman *et al.*, "Components for focused integrated pMUTs for high-resolution medical imaging," *Proc. - IEEE Ultrason. Symp.*, vol. 2, pp. 787–791, 2005.

[6] J. Zahorian *et al.*, "Monolithic CMUT-on-CMOS integration for intravascular ultrasound applications," *IEEE Trans. Ultrason. Ferroelectr. Freq. Control*, vol. 58, no. 12, pp. 2659–2667, Dec. 2011.

[7] G. Gurun *et al.*, "Single-chip CMUT-on-CMOS front-end system for real-time volumetric IVUS and ICE imaging," *IEEE Trans. Ultrason. Ferroelectr. Freq. Control*, vol. 61, no. 2, pp. 239–250, 2014.

[8] R. Chee, A. Sampaleanu, D. Rishi, and R. Zemp, "Top orthogonal to bottom electrode (TOBE) 2-D CMUT arrays for 3-D photoacoustic imaging," *IEEE Trans. Ultrason. Ferroelectr. Freq. Control*, vol. 61, no. 8, pp. 1393–1395, 2014.

[9] T. M. Carpenter, M. W. Rashid, M. Ghovanloo, D. M. J. Cowell, S. Freear, and F. L. Degertekin, "Direct digital demultiplexing of analog TDM signals for cable reduction in ultrasound imaging catheters," *IEEE Trans. Ultrason. Ferroelectr. Freq. Control*, vol. 63, no. 8, pp. 1078–1085, Aug. 2016.

[10] J. Lim, C. Tekes, F. L. Degertekin, and M. Ghovanloo, "Towards a Reduced-Wire Interface for CMUT-Based Intravascular Ultrasound Imaging Systems," *IEEE Trans. Biomed. Circuits Syst.*, vol. 11, no. 2, pp. 400–410, Apr. 2017.

[11] G. R. Lockwood and C. R. Hazard, "Development of small aperture polymer transducers for high frequency imaging," *Proc. IEEE Ultrason. Symp.*, vol. 2, pp. 1717–1720, 1997.

[12] S. J. A. Majerus, S. Mandal, and A. Fleischman, "Catheter-mounted CMOS front-ends for broadband intravascular ultrasonic imaging," *Midwest Symp. Circuits Syst.*, vol. 2017-August, pp. 373–376, Sep. 2017.

[13] J. Wang, Z. Zheng, J. Chan, and J. T. W. Yeow, "Capacitive micromachined ultrasound transducers for intravascular ultrasound imaging," *Microsystems Nanoeng. 2020 61*, vol. 6, no. 1, pp. 1–13, Aug. 2020.