2021 43rd Annual International Conference of the
IEEE Engineering in Medicine & Biology Society (EMBC)
Oct 31 - Nov 4, 2021. Virtual Conference

A Scalable Readout IC Based on Wideband Noise Cancelling for Full-Rate Scanning of High-Density Microelectrode Arrays

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***Abstract*— This paper presents a highly scalable readout IC for high-density microelectrode arrays (MEAs). Although the recent development of large-scale high-density MEAs provides opportunities to achieve sub-cellular neural recording over a wide network area, it is challenging to implement the readout IC that can operate with such MEAs. The requirement of high-speed recording in large-scale arrays induces wideband-noise folding, which makes it challenging to achieve a good noise performance for high-fidelity neural recording. Moreover, for the wideband readout, the major noise contributor changes from the readout circuit to the cell-electrode interface. In this paper, we first show why the interface noise becomes the dominant noise source and elucidate its component that contributes the most: sealing resistance. Then, we propose a new readout circuit structure, which can effectively cancel the wideband interface noise. As a result, the signal-to-noise ratio of input neural spike signals is improved dramatically in all cell-attachment or sealing conditions. Particularly, it is shown that under weakly sealed conditions, the spikes can be detected only when the proposed wideband noise cancellation technique is applied.**

I. Introduction

The microelectrode array (MEAs) have been a crucial platform for scientists and engineers to investigate the nature of neuronal networks or implement brain-machine interfaces. Recent developments in MEA technology have enabled large-scale high-density arrays of microelectrodes to provide high resolution and wide network coverage for neural recording [1]. However, the MEA technology has been scaled at a much slower pace than the CMOS fabrication technology. The number of simultaneously recorded neurons using MEAs has been doubled in approximately seven years [2], while the number of transistors integrated inside a CMOS chip has been doubled every two years. It indicates that the true bottleneck of MEA scaling is not with the fabrication technology.

Rather, the bottleneck arises from the limitation of MEA readout ICs [3]. The conventional readout method (Fig. 1(a)) connects each electrode to a recording channel [4], which typically consists of an AC-coupling capacitor, a low-noise amplifier, a variable-gain amplifier, a low-pass filter, and an analog-to-digital converter. This one-to-one direct wiring between the electrode and recording channel offers the highest possible signal-to-noise ratio (SNR) performance with robust input DC biasing. However, applying the conventional method to high-density MEAs brings about several design issues. Above all, it lays an excessively heavy burden on routing. Since densely packed small-size microelectrodes preclude locating recording channels beneath the electrodes, a large number of routing lines are required to connect the electrodes to recording channels placed on the periphery of the electrode array. The resulting large area occupied by routing lines limits the number of electrodes that can be scaled while maintaining the targeted high density of MEAs. In addition, the area and power consumed by recording channels increase rapidly with the number of electrodes.

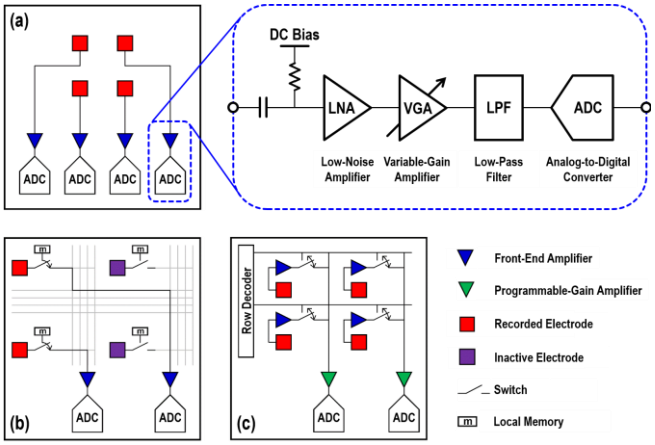

Figure 1. MEA readout methods [3] based on: (a) direct wiring (conventional method) [4], (b) switch matrix [5], and (c) active pixel sensors [6], [7].

To overcome this limitation of the direct-wiring method, the readout structure using a switch matrix (Fig. 1(b)) can be employed [5]. By using multiplexed recording structure, neural signals can be recorded from a large number of electrodes with high spatial resolution. However, since the passive electrodes cannot drive the signal with sufficient speed and strength required to operate the multiplexing switches dynamically, only stationary recording from the preselected set of electrodes is allowed. If we want to achieve full-rate scanning across the entire set of electrodes, the readout approach based on active pixel sensors (Fig. 1(c)) should be used [6], [7]. Here, the active pixel sensor is implemented by placing an extremely small preamplifier under each electrode. Due to this strict area limitation, the noise performance of the preamplifier is far from optimum.

Among different MEA readout approaches, the active-pixel-sensor-based method seems to be the most promising way to maximize scalability, although the SNR performance is compromised mainly due to the significant level of noise generated by preamplifiers. However, as the electrode count

*Research supported in part by the DGIST R&D Program of the Ministry of Science & ICT, Korea, under Grant 21-IJRP-01 and in part by the Future Interconnect Technology Cluster Program of Samsung Electronics, Korea.

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increases beyond a certain limit, another critical noise source starts to make a major contribution. Assume that we target to record from 160,000 electrodes through full-rate scanning. If all pixels are always activated consuming static power, the total power consumption of the readout system will be 160,000 times the consumption by each pixel, which would be too high to avoid harmful effects on living cells. Therefore, the pixel should be dynamically activated only when it is accessed by the recording channel. If 160,000 pixels form the array of 400 × 400, recording channels can be placed on the top and bottom sides of each column. In this arrangement, each channel is supposed to record from a half column of pixels or 200 pixels in a time-multiplexed manner. Assuming 10-kHz recording bandwidth for each pixel, the time window allowed to read out from each pixel becomes as short as 500 ns. It means that once a pixel switch is closed, the neural signal picked up by the corresponding active pixel should settle within 500 ns with high enough accuracy, leading to the requirement of wideband readout circuits. As a result, any band-limiting circuits such as low-pass filters cannot be used in the signal path, and the folding of unfiltered wideband noise occurs when neural signals are sampled in recording channels. Since the thermal noise from readout circuits is one important wideband noise source, we need to keep it as low as possible. However, there is another major wideband noise source that is originated from the cell-electrode interface. In this work, we introduce and analyze the wideband noise from the interface first and then propose a new readout circuit structure, which can mitigate the effect of this interface noise significantly.

II. Noise from Cell-Electrode Interfaces

The electrode itself generates some thermal noise. The electrical properties of the electrode can be well described using a constant-phase model [8], and the real part of the electrode impedance generates Johnson noise. Since the real part of the electrode impedance decreases as the frequency increases, the electrode thermal noise reduces at high frequencies, making it a band-limited noise source.

On the other hand, the cell-electrode interface can be described using two different electrical models depending on the spatial density of MEAs. The first model describes the conventional mechanism of extracellular potential generation. An electrode in a sparse MEA receives multiple electrical signals from multiple neurons' current sources [9]. In this model, obtaining the extracellular potential requires the integration of electric fields caused by the neurons' current sources over distances. A solution resistance is defined from this voltage-current relationship of the model, and its value is a function of electrode dimensions [8].

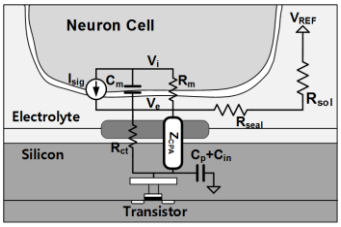

Figure 2. Electrical model of the cell-electrode interface in high-density MEAs [10]–[12].

When it comes to high-density MEAs, a different cell-electrode interface model should be used [10]–[12]. In high-density MEAs, the electrodes are so small and densely packed that each electrode contributes to recording from a single neuron cell or its sub-cell region because a cell or cellular compartment covers or seals the electrode. Fig. 2 shows the electrical model of the cell-electrode interface in high-density MEAs. In this model, a sealing resistance is present between the cell and electrode, and it plays a role of converting the current from the neuron cell to the extracellular voltage at the electrode [10]. As in the patch-clamp experiment, the captured signal quality improves under tighter sealing or better cell attachment conditions.

The values of the solution resistance and sealing resistance show huge differences. For the electrode with an area of several tens of μm^2, the solution resistance value typically ranges from tens of kΩ to hundreds of kΩ, while the sealing resistance value is larger than 1 MΩ [12]–[14]. Therefore, the sealing resistance adds a significantly higher noise floor to the MEA readout system than the solution resistance.

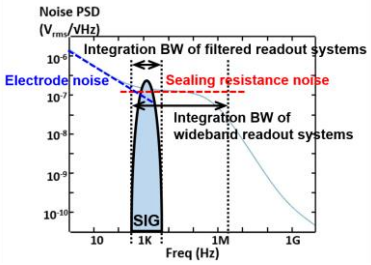

Figure 3. Effects of the sealing resistance noise on filtered MEA readout systems and wideband MEA readout systems.

This high noise floor contributed by the sealing resistance impacts the achievable SNR performance greatly, especially in wideband full-rate-scanning readout systems (Fig. 3). The recording bandwidth of the band-limited or filtered readout system spans mainly over the electrode-noise-dominant region. In contrast, the bandwidth of the active-pixel-sensor-based full-rate-scanning MEA readout system is wide enough to be strongly affected by the sealing resistance noise floor. From the MATLAB simulation using the electrical model of the cell-electrode interface with typical component values, the noise integrated from 300 Hz to 5 kHz for the filtered readout system is 9 μV_{rms}, which is an acceptable level. However, the noise of the wideband readout system having a bandwidth of 2 MHz is turned out to be 87 μV_{rms}, which is excessively high to conduct any successful neural spike recording. It demonstrates that the sealing resistance noise affects wideband full-rate-scanning readout systems significantly while its contribution can be negligible in conventional band-limited recording systems [11]. Therefore, a new method that can suppress the effect of the sealing resistance noise should be introduced to enable highly scalable high-density MEA readout systems.

III. Proposed Highly Scalable Readout IC

A. Active Pixel Design for Wideband Noise Cancellation

The sealing resistance noise comes into the recording circuit in conjunction with the input neural signal, and thus it is not straightforward to distinguish it from the input signal. Considering that its frequency range is much wider than that of the input signal, we propose a new front-end circuit structure that performs two-path asymmetric high-pass filtering and subsequent subtraction (Fig. 4(a)). Two high-pass

filters with different cutoff frequencies are implemented within a pixel. The high-pass filter with 300-Hz cutoff passes the signal together with noise, and the other high-pass filter with 10-kHz cutoff passes only the wideband noise. These two filter outputs are then subtracted in the half-column recording channel to cancel the wideband noise from the sealing resistance. To minimize the area consumption, the capacitors in high-pass filters are realized by using the inherent electrode capacitance, and the resistors are implemented by using switched capacitors. Note that platinized Pt-black electrodes can offer about 10-pF capacitance per 1-μm^2 area [8], [15]. Although the electrode capacitance value can vary significantly due to process variations, the cutoff frequency can be accurately adjusted by tuning the switched-capacitor operation frequency. Two input electrodes are placed in a mosaic configuration to obtain the highest possible input correlation.

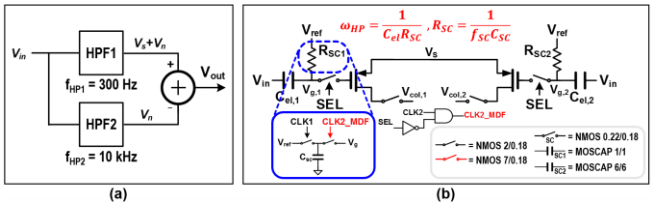

Figure 4. Active pixel circuit for wideband noise cancellation: (a) block diagram, (b) circuit schematic diagram.

Fig. 4(b) shows the schematic diagram of the active pixel circuit. The clock frequency for switched-capacitor resistors is set to 10 MHz so that the consistent equivalent resistance can be seen by all frequency components of the input signal and noise up to 2 MHz. The resistance values required to generate 300-Hz and 10-kHz cutoff frequencies are 5 MΩ and 250 kΩ, corresponding to the switched capacitance values of 20 fF and 400 fF, respectively. The switched capacitors are implemented using MOS capacitors. The switches at the gates of input transistors are included to minimize the crosstalk between pixels. Since the input transistor operates as a large coupling capacitor that causes crosstalk when the pixel-selection switch at its drain terminal is turned off, the input transistor needs to be disconnected from the input node to prevent the signal contamination due to crosstalk between pixels.

B. Half-Column Recording Channel Design

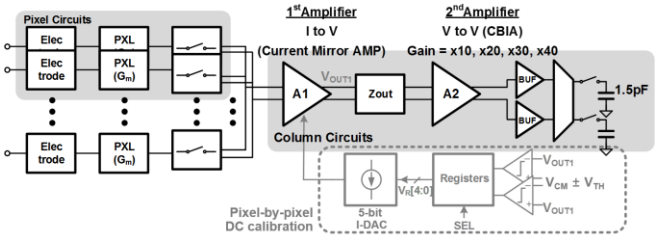

Figure 5. Block diagram of the half-column recording channel.

Fig. 5 presents the block diagram of the half-column recording channel. To achieve high-speed switching between pixels in the presence of large parasitic capacitances due to long wires running along the half-column, the current-mode readout is employed for the 1st stage amplification. In the 1st stage amplifier, the current-mirror-based amplification is performed with a gain of 4. The current-bleeding technique is implemented using I_{BLD} to reduce the DC current consumption of current mirror stages, and bandwidth-enhancement loops [6], [7] are formed by M_{SF1} and M_{SF2} for fast settling. The 1st stage amplifier draws a sufficiently large DC current to lower the circuit thermal noise floor. However, since the pixel circuits operate dynamically with sharing the DC current of the 1st stage amplifier in the half-column recording channel, the total power consumption does not grow so rapidly as the number of electrodes in the MEA increases. After the current amplification, the current-to-voltage conversion is conducted by the output resistance (R_{OUT}) of 120 kΩ. In addition, the output capacitance (C_{OUT}) of 500 fF is used to filter out the noise at excessively high frequencies beyond 2 MHz, which is the target bandwidth of the recording channel. The total gain of the 1st stage amplifier is 100. The circuit schematic diagram of the 1st stage amplifier is shown in Fig. 6.

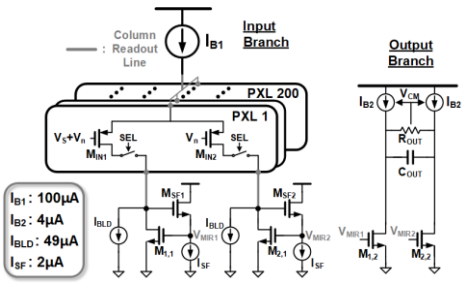

Figure 6. Circuit schematic diagram of the 1st stage amplifier in the half-column recording channel.

The 2nd stage amplifier in the recording channel is based on a current-balancing instrumentation amplifier (CBIA) structure [16]. Since the CBIA operates in an open-loop manner, it can achieve a wide bandwidth with low power consumption, while the gain of the amplifier can be reliably set by the ratio between two resistors. The 2nd stage amplifier gain is designed to be programmable among 10, 20, 30, and 40. The sampling stage that follows the 2nd stage amplifier consists of buffers, switches, and sampling capacitors. The amplifiers used in the buffers are conventional Miller-compensated two-stage amplifiers. The value of the sampling capacitors is set to 1.5 pF, considering kT/C noise.

In addition to the main recording channel circuit, a pixel-by-pixel DC calibration circuit should be implemented to deal with DC offset variations across pixels (Fig. 5). The charge injected by gate switches, switched-capacitor resistors, and pixel-selection switches at input transistor drain terminals is discharged slowly through large sealing resistances. Therefore, the amount of injected charge and its discharging speed are different from pixel to pixel, leading to varying DC offsets across pixels. Therefore, the DC calibration circuit is required to compensate for these DC offsets so that the saturation of the recording channel can be avoided. The DC calibration circuit monitors the voltage at the 1st stage amplifier output when connected to each pixel. If the output voltage exceeds the predetermined threshold when connected to a certain pixel, the compensation data stored in the registers for that specific pixel is updated. The 5-bit current-mode digital-to-analog converter (I-DAC) is then controlled by the stored compensation data to compensate for the DC offset of the corresponding pixel. The I-DAC is connected in parallel with I_{BLD} current sources in a differential manner (Fig. 6).

IV. Implementation Results

The proposed recording system, including 200 active pixels and a half-column recording channel, is implemented using 28-nm CMOS technology, and transient simulations are carried out using the Cadence Spectre to verify its recording operation and performances. Three different sealing resistance values (1 MΩ, 5 MΩ, and 10 MΩ) are used for simulation. The electrical model of the cell-electrode interface shown in Fig. 2 is used to construct the input source network of the recording system. Although the constant-phase electrode model can be constructed using Spectre codes, it cannot be used for transient simulations. Thus, an equivalent RC model having similar noise and frequency characteristics is used instead.

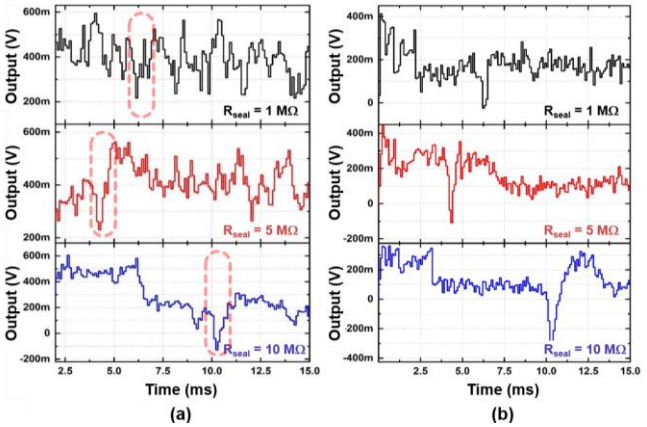

Figure 7. Recording output waveforms obtained from transient simulations for three different sealing resistance conditions (1 MΩ, 5 MΩ, and 10 MΩ): (a) without wideband noise cancellation, (b) with wideband noise cancellation.

Fig. 7(a) shows the output waveforms when the proposed wideband noise cancellation technique is not applied. In this simulation, the 10-kHz high pass filter in the active pixel is removed, and the corresponding input node is connected to a suitable DC voltage. When the sealing resistance is 1 MΩ, the neural spike cannot be distinguished from the noise. For the sealing resistances of 5 MΩ and 10 MΩ, the achieved recording SNR improves slightly, but it is still low. Fig. 7(b) shows the output waveforms obtained with applying the proposed wideband noise cancellation technique. It is obvious that the SNR performance improves significantly when this technique is applied. For any values of the sealing resistance, the neural spikes are clearly discernible at the output. The SNR increases when the value of sealing resistance increases because the signal magnitude is proportional to the sealing resistance, while the noise amplitude is proportional to the square root of the sealing resistance.

V. Conclusion

The MEA technology is being scaled incessantly but at a rather slow pace. One important factor that results in such slow development is the limited scalability of the MEA readout IC because reading out from the large-scale high-density MEA is a challenging task. To operate with the large-scale MEA, the readout IC should be able to record neural signals from a large number of electrodes through high-speed or wideband recording. Considering the adverse effect of the wideband noise folding on the achievable SNR performance of high-speed readout IC, the circuit thermal noise performance should be improved significantly by consuming more power and area. However, to operate with the densely packed electrodes at the same time, increasing power and area consumption is not a viable option due to the risk of cell damage and unavailability of the large implementation area. Moreover, as the recording bandwidth of the readout IC increases for full-rate scanning of large-scale MEAs, the wideband noise from the sealing resistance in the cell-electrode interface becomes more important than the thermal noise from the readout IC and degrades the SNR performance of the wideband readout IC seriously. In conclusion, it is extremely challenging for the readout IC to satisfy the requirements of highly scalable recording and high-density recording simultaneously.

In this work, to overcome this limitation, we present a new readout IC structure with wideband noise cancellation. Implemented in a 28-nm CMOS process, it is demonstrated that the proposed readout IC can achieve dramatically improved SNR performance in all cell-attachment conditions with various sealing resistance values. Importantly, recorded neural spikes in the weak sealing conditions can be distinguished from the noisy background only when the wideband noise cancellation technique is applied to the readout IC.

References

[1] G. Hong and C. M. Lieber, "Novel electrode technologies for neural recordings," *Nat. Rev. Neurosci.*, vol. 20, pp. 330–345, Mar. 2019.

[2] I. H. Stevenson and K. P. Kording, "How advances in neural recording affect data analysis," *Nat. Neurosci.*, vol. 14, no. 2, pp. 139–142, Feb. 2011.

[3] M. E. J. Obien *et al.*, "Revealing neuronal function through microelectrode array recordings," *Front. Neurosci.*, vol. 8, article 423, Jan. 2015.

[4] R. Segev, G. Goodhouse, J. Puchalla, and M. J. Berry, "Recording spikes from a large fraction of the ganglion cells in a retinal patch," *Nat. Neurosci.*, vol. 7, no. 10, pp. 1155–1162, Oct. 2004.

[5] U. Frey *et al.*, "Switch-matrix-based high-density microelectrode array in CMOS technology," *IEEE J. Solid-State Circuits*, vol. 45, no. 2, pp. 467–482, Feb. 2010.

[6] B. Eversmann *et al.*, "A 128 × 128 CMOS biosensor array for extracellular recording of neural activity," *IEEE J. Solid-State Circuits*, vol. 38, no. 12, pp. 2306–2317, Dec. 2003.

[7] B. Eversmann *et al.*, "A neural tissue interfacing chip for in-vitro applications with 32k recording / stimulation channels on an active area of 2.6 mm^2," in *Proc. Eur. Solid-State Circuits Conf.*, Sept. 2011, pp. 211–214.

[8] W. Franks *et al.*, "Impedance characterization and modeling of electrodes for biomedical applications," IEEE Tran. Biomed. Eng., vol. 52, no. 7, pp. 1295–1302, July. 2005.

[9] R. Plonsey and R. C. Barr, *Bioelectricity: A Quantitative Approach*, 3rd ed., Boston, MA, USA: Springer, 2007, pp. 223–231.

[10] N. Joye, A. Schmid, and Y. Leblebici, "A cell-electrode interface noise model for high-density microelectrode arrays," in *Proc. Ann. Int. Conf. IEEE Eng. Med. and Biol. Soc.*, Sept. 2009, pp. 3247–3250.

[11] J. Guo, J. Yuan, and M. Chan, "Modeling of the cell-electrode interface noise for microelectrode arrays," *IEEE Trans. Biomed. Circuits Syst.*, vol. 6, no. 6, pp. 605–613, Dec. 2012.

[12] C. M. Lopez *et al.*, "A multimodal CMOS MEA for high-throughput intracellular action potential measurements and impedance spectroscopy in drug-screening applications," *IEEE J. Solid-State Circuits*, vol. 53, no. 11, pp. 3076–3086, Nov. 2018.

[13] S. Ingebrandt, C.-K. Yeung, M. Krause, and A. Offenhäusser, "Neuron-transistor coupling: interpretation of individual extracellular recorded signals," *Eur. Biophys. J.*, vol. 34, no. 2, pp. 144–154, Mar. 2005.

[14] S. Martinoia *et al.*, "Cultured neurons coupled to microelectrode arrays: circuit models, simulations and experimental data," *IEEE Trans. Biomed. Eng.*, vol. 52, no. 5, pp. 859–864, May 2004.

[15] D. A. Robinson, "The electrical properties of metal microelectrodes," *Proceedings of the IEEE*, vol. 56, no. 6, June 1968

[16] R. F. Yazicioglu, P. Merken, R. Puers, and C. Van Hoof, "A 200 µW eight-channel EEG acquisition ASIC for ambulatory EEG systems," *IEEE J. Solid-State Circuits*, vol. 43, no. 12, pp. 3025–3038, Dec. 2008.