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Thermoelectric Energy Harvesting for Implantable Medical Devices

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***Abstract*— A thermoelectric energy harvesting system is proposed to supplement the primary power supply of an implantable medical device. A low-power synchronous boost converter capable of boosting 10mV input voltage to 1V output voltage is designed in a 180nm CMOS process. To increase the charging speed, a maximum power transfer scheme is utilized. The harvester delivers up to 10µW power with a minimum temperature gradient of 1-degree, which results in a power efficiency over 40%.**

***Clinical Relevance*— The use of this technology could enhance the longevity of battery-operated implanted medical devices by reducing the possibility of invasive battery replacement surgery.**

I. Introduction

The healthcare industry continues to increase its use of implantable medical devices (IMDs) for lifesaving therapeutic and diagnostic monitoring functions. Long term trending and automatic remote RF transmission of patient data can provide early detection of serious medical conditions leading to timely physician intervention. These devices use batteries that eventually run out of charge and often need surgical replacement, which can be costly and taxing to patients [1],[2]. This research seeks to reduce the frequency at which batteries in IMDs need replacement by supplementing the implant's battery power with power harvested from ambient sources. More specifically, thermoelectric energy harvesting is targeted as the alterative power source. By using a thermoelectric generator (TEG) in the presence of a temperature gradient, an open-circuit voltage develops across the two plates of the TEG. Since natural temperature gradients exist between the inner side of the skin and the interior of the body, thermoelectric energy harvesting is a viable source of additional power for implants deployed just below the skin.

The proposed circuitry is designed in way to interface with an implantable cardiac monitor (ICM) such as Biomonitor (manufactured by Biotronik), which is a subcutaneous implant used for continuous cardiac health monitoring [3]. Furthermore, the TEG selected for this research is the 1MC04-048-05_TEG from TEC Microsystems due to its small size (8 mm x 8 mm x 1.6 mm) and reasonable voltage development (19.2 mV/ºC) [4] with low source resistance (3Ω). The proposed energy harvesting system includes a boost converter with dual-mode control designed in a 180 nm CMOS process.

II. System Overview

A. Modes of Operation

The system designed uses a DC-DC boost converter controlled with voltage-mode feedback outlined in [5]. In addition to feedback used to regulate the output voltage to a constant reference, the system uses an additional mode of operation upon startup. This additional mode of operation is referred to as maximum-current mode and transfers maximum power to the output. To distinguish between the two modes of operation, the mode making use of voltage-mode control will be referred to as constant-voltage mode. As per the maximum power transfer theorem, the maximum amount of power transfers to the load when the source and load impedances are equal [6]. Furthermore, the time it takes to charge a capacitor to a certain voltage can be given by

$$T = CV/I \tag{1}$$

which decreases as current *(I)* increases. Thus, if the circuit maximizes the current charging the output capacitor (here the storage capacitor), the time needed to charge the capacitor to voltage *(V)* is minimized.

To achieve maximum power transfer, the circuit performs an impedance match by regulating the harvester input voltage to one-half the value of the TEG's open-circuit voltage (OCV). The regulation circuitry used in the maximum-current mode is shared with the constant-voltage mode. The implementation of the maximum-current mode requires additional circuitry to the traditional voltage-mode control scheme. Such blocks include a circuit capable of sampling the TEG's open-circuit voltage, multiplexers along the control path, a hysteretic comparator to set the mode of operation, and source-followers to buffer high-impedance nodes.

B. System Design

High-level system block diagram is shown in Fig. 1. The DC-DC boost converter steps up the low-voltage input level from the TEG to the ICM's supply voltage, which is 1V. This application uses a synchronous boost converter to enhance efficiency of the harvester, which requires additional timing logic in the form of a non-overlapping clock generator circuit.

The pulse-width modulation (PWM) controller implements both operation modes and takes a clock signal from the oscillator. A hysteretic comparator's output sets the mode of operation in the circuit by comparing the output voltage to a reference. The PWM controller's components are illustrated in Fig. 2.

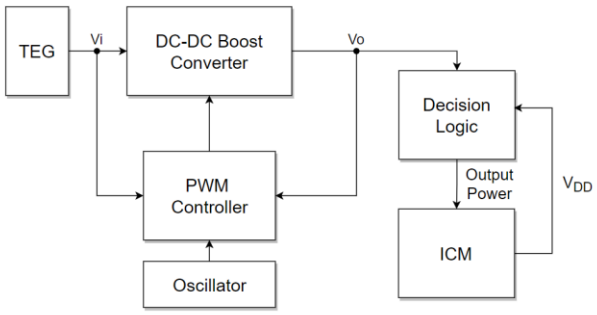

Figure 1. High-level System Block Diagram

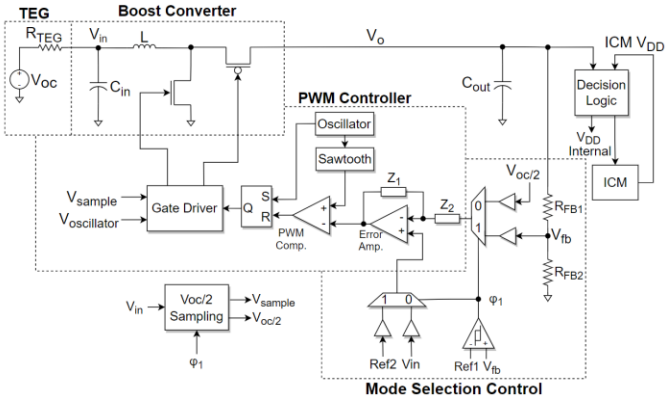

Figure 2. Control System Diagram

The decision logic circuit in Fig. 2 selects either the boost converter's output (V_O) or the fixed battery (V_{DD}) to feed into the ICM as a power source. The decision logic circuitry also determines the power supply of the harvester, which is also either V_{DD} or V_O. This ensures that both the ICM and harvester have access to power in all conditions. The selections result from comparisons between reference voltages and the boost converter's output voltage with hysteretic comparators. Hysteresis was added to the comparators to prevent oscillations around the trigger point. The algorithm used for power supply and mode selection is shown in Fig. 3.

III. Control Circuitry

A. Oscillator

The PWM controller is enabled using an oscillator which is designed based on the low-power relaxation oscillator proposed in [7]. It consists of startup circuitry, a Wilson current mirror, current-mode comparator, and output buffers. The output feeds back to the gate of an NMOS switch (M_1) that discharges a capacitor to ground when turned on. The design produces oscillations with inherently low duty cycles, which supplanted the need to have a one-shot clock generator. This is because a 50% duty cycled clock is not needed in this scheme: only a low duty cycle signal is necessary.

The schematic for the oscillator is shown in Fig. 4. The duty cycle of the output clock signal is governed by the size of M_1 and the size of C_{INV}. Increasing the size of M_1 and/or C_{INV} increases the duty cycle. The period of the oscillations is approximated as

$$T = RC + \tau \qquad (2)$$

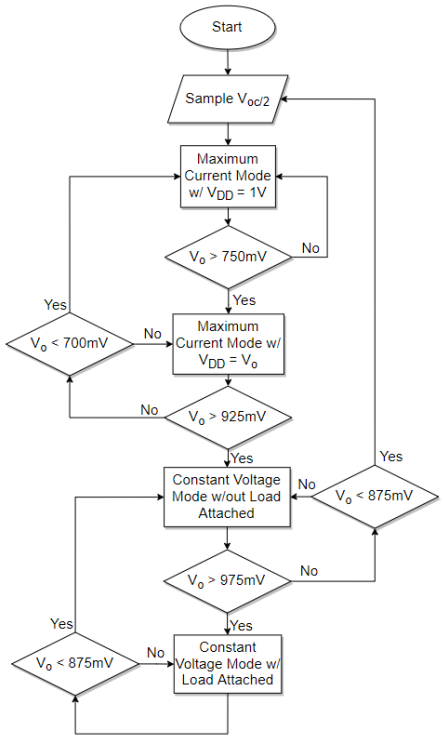

Figure 3. Decision Logic Algorithm

$$\tau \propto \frac{V_{DD}\, C_{INV}}{I_{BIAS}} \qquad (3)$$

The oscillator produces duty cycles ranging from 0.27% to 1.02% across the range of expected V_{DD} values. The frequency varies from 46.2 kHz to 57.7 kHz, which was selected to be high enough to ensure the boost converter operates in continuous-conduction mode.

B. Error Amplifier

The error amplifier is implemented as an operational amplifier with negative feedback to produce a low-pass filter. Its inputs connect to the output of two multiplexers that select the signals to compare depending on the mode of operation. For maximum-current mode, the inverting terminal of the error amplifier is connected to the $V_{OC/2}$ voltage through an impedance Z_2, as shown in Fig 2. The $V_{OC/2}$ voltage is the result of sampling the TEG's open-circuit voltage, using a voltage divider to cut the voltage in half, and storing the voltage on a capacitor. The non-inverting terminal connects to the input voltage V_{in} during maximum-current mode. During constant-voltage mode, the inverting terminal is connected to the feedback voltage V_{fb} through Z_2, and the non-inverting input is connected to a target reference. This reference voltage determines the target output voltage for the loop.

The amplifier designed has a DC gain above 80dB and unity-gain phase margin above 15º for the range of V_{DD} values expected (700mV to 1V). This ensures accuracy and stability of the regulation loop. The topology used for the error amplifier design is a 2-stage Miller op-amp with PMOS input pair devices.

Voltage-mode control may have stability issues when not properly compensated. A standard compensation scheme described in [8] is utilized to help stabilize the system. Fig. 5 illustrates this control scheme.

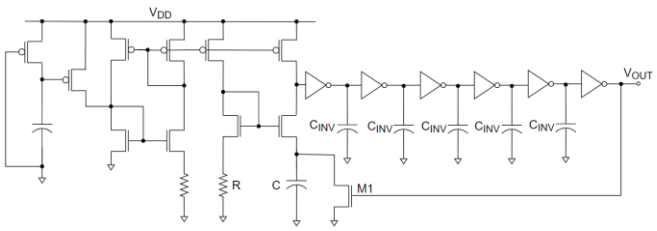

Figure 4. Oscillator Schematic

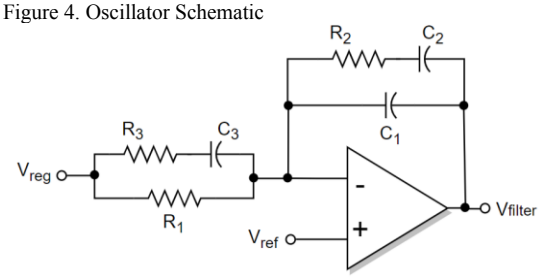

Figure 5. Compensation Approach

C. Comparator

The comparator in the control loop creates the PWM signal by comparing the amplified error with a sawtooth waveform. The result is a duty cycle modulated signal, which is used to switch the transistors in the boost converter to control the gain and input impedance of the boost converter. The circuit topology used in this application is inspired by [9] but is modified to better suit this application. The PWM comparator circuit uses a fully-differential first stage with large resistors connecting the drain and gate of the load transistors. Using resistors increases the gain, compared to just using diode-connected devices. The second stage is a push-pull class AB amplifier to provide additional gain to the circuit. Having higher gain leads to increased speed, which is important for this application due to the necessity of using high duty cycle values. This block also uses a higher bias current than other blocks to increase speed at the cost of higher power consumption.

D. Hysteretic Comparator

A hysteretic comparator compares two voltages but adds hysteresis using positive feedback. If the voltage at the output is originally a digital low, the non-inverting input must exceed the inverting input by an amount equal to the hysteresis value. The hysteretic comparator for this application is designed to have symmetric hysteresis of 2.5mV. The reason the hysteresis value is this low is due to the use of the divided feedback voltage in the circuit. The hysteretic comparators handle voltages multiplied by β, which is 1/10 in this application. Since the division factor is 10, the 2.5mV hysteresis represents 25mV of hysteresis with the signals it compares. The circuit designed is derived from [10].

E. Gate Driver

The MOSFETs in the boost converter are designed to be large devices to reduce conduction losses when turned on. The capacitance and switching losses increase with switch size, so there exists an upper limit for the benefit gained from increasing transistor width. Furthermore, since the capacitance of each switch is large, a driver circuit is used to minimize the delay in switching the NMOS and PMOS devices. This is implemented using serially connected inverters sized using stage ratios based on the logical effort needed to drive the gate capacitors. Additionally, the gate driver circuit performs the necessary logical operations on the PWM signal. One such operation is implementing maximum duty cycle logic to prevent signals from having a 100% duty cycle. The maximum duty cycle logic is performed with the circuit shown in Fig. 6(a).

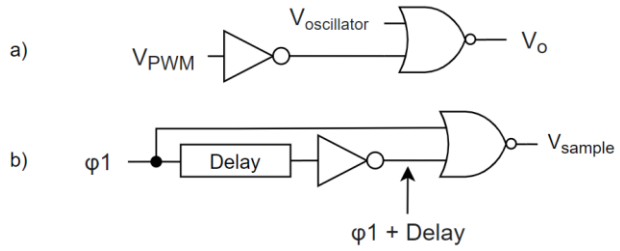

Figure 6. a) Maximum Duty Cycle Logic Circuit b) Voc/2 Sampling Circuit

F. Open-circuit Voltage Sampling

The maximum-current mode of operation regulates the input voltage to the value of the TEG's open-circuit voltage divided by two. To do this, the open-circuit voltage must be sampled. A modified one-shot clock generator is used to produce a short pulse to switch an NMOS transistor connected to the middle node of a 1:1 voltage divider and a storage capacitor. The node connected to the storage capacitor is taken to be the reference needed to regulate the circuit's input voltage to $V_{OC}/2$. The one-shot fires when the mode of operation changes from constant-voltage mode to maximum-current mode to update the reference. The one-shot also fires upon startup. Fig. 6(b) shows the one-shot circuit's logical components. The sampling one-shot pulse is plotted alongside the mode value in Fig. 7.

The proposed sampling method proves effective but limiting. The leakage from the storage capacitor is non-negligible, meaning the impedance match gets worse over time. An alternative method that may be explored in the future is to use an up-counter to form a periodic one-shot.

IV. Layout and Results

The final layout of the circuit is shown in Fig. 8. The total chip area is 1.06mm x 1.06mm, including I/O pads, and is fitted for a 3mm x 3mm package with 12 leads.

The results of simulating the 1 ºC temperature gradient case are shown in Fig. 9. This represents the worst-case scenario designed for in this application because 1 ºC is the lowest value for the expected range of temperature gradients. The input voltage shows the impedance matching performed in maximum-current mode. The open-circuit voltage is 19.2mV, so the expected input voltage in this mode is 9.6mV. The V_{in} value is near this value for the beginning of the circuit's operation and begins to decline due to reference leakage.

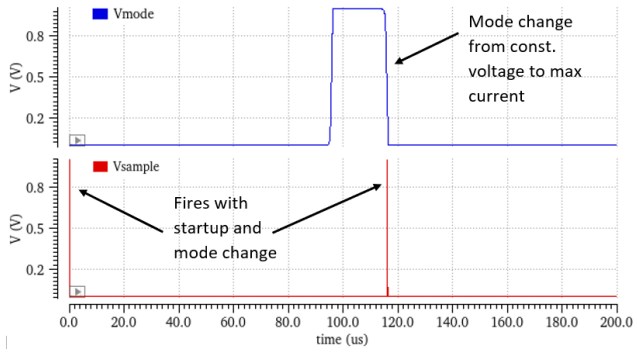

Figure 7. Voc/2 Sampling Waveforms

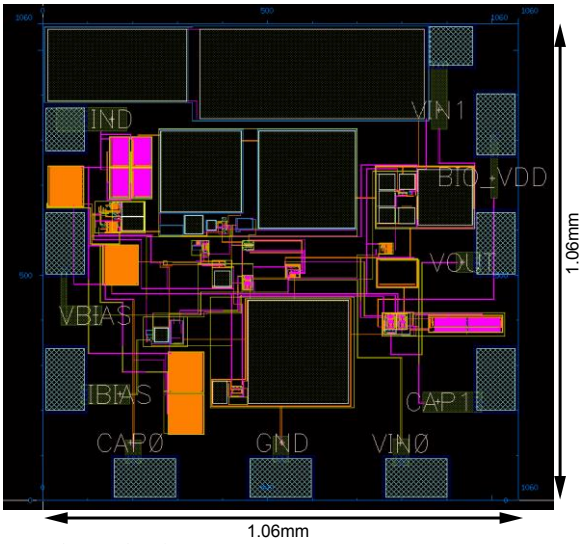

Figure 8. Thermoelectric Energy Harvester Layout

Furthermore, the transient simulation is performed with a load current of 10µA since most of the ICM's operations require less than 10µW of power for a V_{DD} of 1V. The output voltage nears the 1V steady-state condition but begins to drop when the ICM is suddenly connected since there is not enough system bandwidth available to fully support the transient. The IC still delivers harvested power to the ICM during this time and requires no additional support from the ICM to sustain operation. Thus, the supplementary harvested power is provided to the IMD.

Power conversion efficiency is an important metric in evaluating the performance of a boost converter. The equation for power conversion efficiency is given by

$$\eta = \frac{P_{OUT,max}}{P_{IN}} \cdot 100\%. \quad (4)$$

This value is 40.9% for the proposed power harvester. This may seem low for a boost converter, but it is a typical for ultra-low power applications. This value includes the power consumption of the control circuitry since the IC powers these blocks in addition to providing power to the load. In addition to the power conversion efficiency, the power consumption of individual circuit blocks is shown in Table 1.

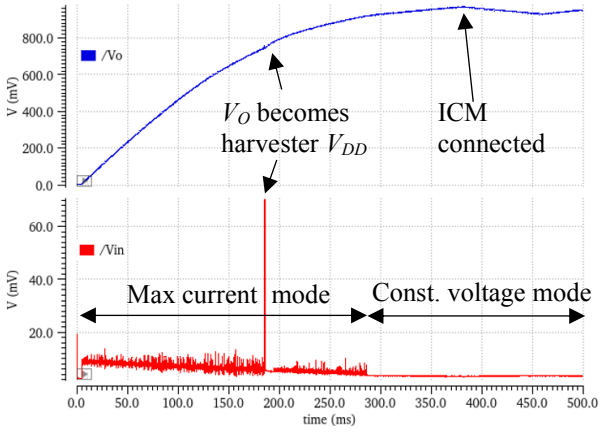

Figure 9. Transient Results – Spike in V_{in} due to Changing IC V_{DD} to V_o

TABLE I. POWER CONSUMPTION

Circuit Element	*1 ºC Case*
Control circuitry	4.26 µW
P switch	2.89 µW
N switch	6.19 µW

V. CONCLUSION

The use of thermoelectric energy harvesting was explored to supplement the primary power supply of a biomedical implant. The proposed work implements a low-power synchronous boost converter capable of boosting 10mV input voltage to 1V output voltage. Maximum power transfer was achieved using digital logic and the proposed sample-hold technique. The harvester delivers up to 10µW power with a minimum temperature gradient of 1-degree, which results in a power efficiency over 40%.

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