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AC-Coupled CMOS Neural Amplifier Optimized for Low Level Distortions over Full Bandwidth

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***Abstract*— Multichannel CMOS neural amplifiers use high-value pseudoresiststors to realize high-pass filters that remove the electrode DC voltages. The pseudoresistors are highly nonlinear and can cause large distortion for signal frequencies near the filter cutoff frequency. Here we present test results of a prototype CMOS neural amplifier with greatly improved pseudoresitor linearity. The THD levels below 1.1% for 10 mVpp input signal have been achieved.**

***Clinical Relevance*— The presented preamplifier is foreseen for recording extracellular signal using high density multielectrode arrays.**

I. INTRODUCTION

Modern neural recording systems use multichannel ASICs to amplify signals from hundreds or thousands of microelectrodes in parallel. The amplifiers routinely use AC coupling to remove the DC electrode voltages. Most designs take advantage of the architecture proposed by Harrison & Reid [1] in which the high-pass filter pole is set by product of the feedback resistance and capacitance (Fig. 1). Due to silicon area restrictions, the resistors are realized by using MOSFET transistors biased in deep subthreshold region. However, such pseudoresistors suffer from poor linearity which is primarily caused by variation of the V_{gs} voltages of the transistors during signal amplification. These effects result in large nonlinear distortions when the signal amplitude is large (a few mV) and its frequency is close to the cut-off frequency. In this work, we present the measurements of a prototype CMOS preamplifier designed specifically for amplification of the extracellular neuronal signals with very low distortion.

II. METHODS

The prototype ASIC was designed in 0.18 µm SOI CMOS technology and comprises 14 identical AC-coupled preamplifiers. We used a slightly modified telescopic cascode architecture that allows the V_{gs} value for the transistors forming the pseudoresistor to be independent of the output signal. The cutoff frequency of the AC-coupling circuit can be set between 0.1 Hz and 10 Hz and the gain is fixed at 26 dB; the circuit is planned to be combined with the second amplification stage to achieve total gain of ~40 dB. Details of the circuit design and analysis of circuit distortion and noise have been presented in [2].

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III. RESULTS

The measured characteristics of THD-vs-frequency measured for 14 channels are shown in Fig. 1. As expected, they exhibit a maximum near the lower cut-off frequency. The maximum increases with signal amplitudes and reaches a value of ~1.1% for the largest perceived signal amplitude (10 mV pp). These results are consistent with numerical simulations [2] and the channel-to-channel variation is even lower compared to Monte Carlo simulation of matching.

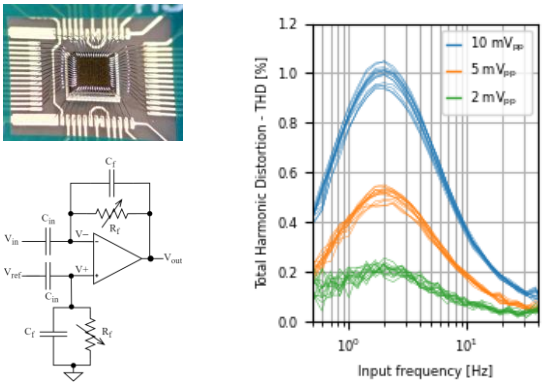

Figure 1. Left: Photograph of the ASIC mounted on the evaluation board and simplified schematic of the AC-coupled neural amplifier; Right: Measured THD vs. frequency for AC-coupled neural amplifier (with 1 Hz cutoff frequency) and various input signal amplitudes.

IV. DISCUSSION & CONCLUSION

The measurements results confirm that the proposed preamplifier can amplify the full spectrum of signals recorded by extracellular electrodes (1 Hz - 10 kHz, amplitudes up to 10 mV pp) with THD on the order of 1% or lower. To our knowledge, such performance has not been reported for any of the CMOS neural amplifiers described in the literature. The small silicon area of the preamplifier (0.0046 mm^2) makes it suitable for future neuroelectronic interfaces with very large number of channels [3].

REFERENCES

[1] R. R. Harrison et al., "A low-power low-noise CMOS amplifier for neural recording applications," IEEE J. Solid-State Circuits, vol. 38, no. 6, pp. 958–965, Jun. 2003.

[2] B. Trzpil-Jurgielewicz, W. Dąbrowski, and P. Hottowy, "Analysis and Reduction of Nonlinear Distortion in AC-Coupled CMOS Neural Amplifiers with Tunable Cutoff Frequencies," Sensors, vol. 21, no. 9, p. 3116, Apr. 2021.

[3] J. J. Jun et al., "Fully integrated silicon probes for high-density recording of neural activity," Nature, vol. 551, pp. 232-236, 2017.